Remarks/Arguments:

The present invention relates to a digital signal receiver which includes a signal generator and a base-band transform circuit. Specifically, a frequency divider divides a reference signal and a frequency multiplier multiplies the output of the divider by a multiplier value. The output of the frequency multiplier is a product of the output signal of the divider and the multiplier value of the frequency multiplier.

On page 5, the Official Action rejects claims 1-10 under 35 U.S.C. §112 as failing to comply with the enablement requirement. Specifically, in claim 1, Applicants have replaced "*a magnitude of the frequency multiplier*" with "*a multiplier value of the frequency multiplier*". Furthermore, Applicants have replaced the recitation of "*the frequency*" with the recitation of "*a frequency*". Withdrawal of the 112 rejection is respectfully requested.

On page 6, the Official Action rejects claims 1-10 under 35 U.S.C. §103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) in view of Hayashi (U.S. Patent No. 6,075, 829). It is respectfully submitted, however, that the claims are patentable over the art of record for the reasons set forth below.

Applicants' claim 1 is different than Hayashi, because Applicants recite a **frequency multiplier** whereas Hayashi teaches a **heterodyning multiplier**. A frequency multiplier is functionally different than a heterodyning multiplier. Specifically, a frequency multiplier produces a **product between** an input frequency (**multiplicand**) and a multiplier value of the frequency multiplier (**multiplier**). In contrast, a heterodyning multiplier produces two sinusoids in which the frequencies are the **sum** and the **difference**.

Support for the difference between a heterodyning multiplier and frequency multiplier can be found in Tunick (US Patent 2,407,212). Specifically, col. 2 of Tunick teaches a received wave being heterodyned to produce a difference frequency and then frequency multiplied to produce a product frequency ("*difference frequency is amplified in an intermediate frequency amplifier 506...the difference frequency may be made equal to one megacycle...514 may include a frequency multiplier so that the radiated frequency may be some multiple of the output*"). This feature is shown in Fig. 1 of Tunick, wherein a 600 Mc signal and 599 Mc signal are heterodyned by converter 502 to produce a difference signal of 1 Mc (heterodyne multiplier).

The difference signal of 1 Mc (multiplicand value) is then multiplied by frequency multiplier 508 with a value of 3 (multiplier value), to produce a frequency of 3 Mc (product).

Hayashi teaches a digital broadcast receiver. Specifically, Hayashi teaches a reference signal that is divided in frequency and then outputted to a heterodyning multiplier.

Applicants' invention, as recited by claim 1, includes a feature which is neither disclosed nor suggested by the art of record, namely:

> **... a frequency multiplier wherein an output frequency of the frequency multiplier is a product of a multiplicand value which is the divided frequency of the first reference signal produced by the frequency divider and a multiplier value of the frequency multiplier ...**

Claim 1 relates to a frequency multiplier which produces an output frequency which is the product between an output frequency (multiplicand) of a frequency divider and a value (multiplier) of the frequency multiplier. This feature is found in the originally filed application on page 3, and furthermore Fig. 1. No new matter has been added.

Fig. 1 of Hayashi shows frequency divider 35 and heterodyning multiplier 11. In Hayashi's heterodyning multiplier, two sinusoids are multiplied together in a heterodyning procedure wherein the output produces two new sinusoids with frequencies at the sum **(F1 + F2)** and the difference **(F1 - F2)** of the input frequencies **(F1, F2)**.

Applicants' claim 1 is different than Hayashi because of a **frequency multiplier** which produces an output frequency which is the product of the frequency divider output (multiplicand) and a value (multiplier) of the frequency multiplier. For example, assuming the frequency divider output (multiplicand) is **(1,000 Hz)** and the value of the frequency multiplier (multiplier) is **(3)**, then the output of the frequency multiplier would be the **product (multiplicand*multiplier=product) (1,000 Hz)*(3)=(3,000 Hz)**. An example illustration of the comparison between Applicants' frequency multiplier as recited in claim 1 and Hayashi's heterodyning multiplier is shown in the enclosed explanatory figure. Thus, Applicants frequency multiplier as cited in claim 1 produces a product between the frequency output of the frequency divider (multiplicand) and the multiplier value of the frequency multiplier (multiplier). Therefore, the combination of Hayashi's heterodyning multiplier with AAPA would not teach the

feature of Applicants' claim 1 (a frequency multiplier is not the same as a heterodyning multiplier).

It is because Applicants include the feature of "*a frequency multiplier wherein an output frequency of the frequency multiplier is a product of a multiplicand value which is the divided frequency of the first reference signal produced by the frequency divider and a multiplier value of the frequency multiplier*", that the following advantages are achieved. An advantage is to reduce the frequency of the signal that is input to the frequency multiplier, thus reducing the buffer current that is needed. Accordingly, for the reasons set forth above, claim 1 is patentable over the art of record.

Claims 2-10 include all of the features of claim 1 from which they depend. Thus, claims 2-10 are also patentable over the art of record for the reasons set forth above.

In view of the amendments and arguments set forth above, the above identified application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

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Enclosure: Explanatory Figures

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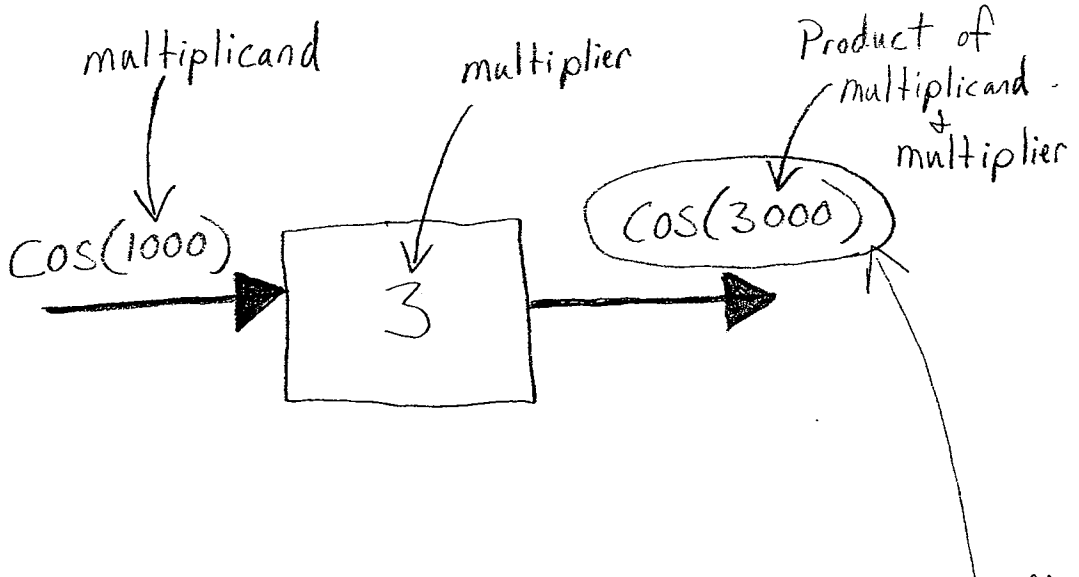
Ex

Applicants

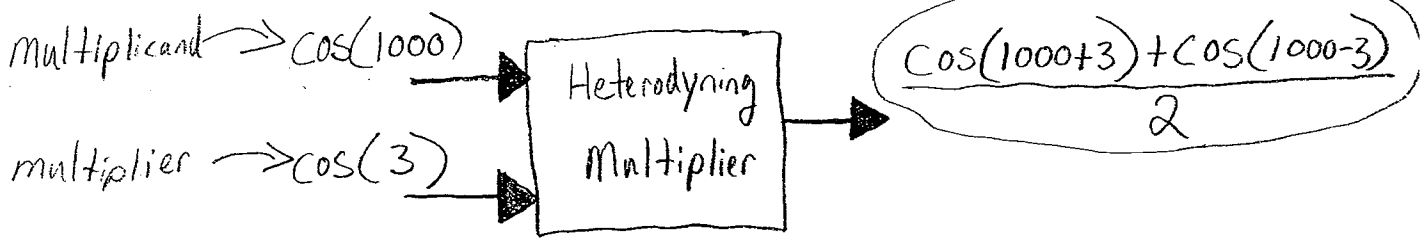


Not Equal

≠

Ex

Hayashi



Comparison

Applicants

multiplicand = 1000

multiplier = 3

Hayashi

multiplicand = cos(1000)

multiplier = cos(3)

EXPLANATORY FIGURE - DO NOT ENTER